**Proposal of internship**

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| Title | Base Band circuits design for ADPLL Synthesizers in nanometer technologies |
| Study Level | Masters student |
| Duration | ~6 months |

Huawei Technologies is a leading global information and communications technology (ICT) solutions provider. Driven by a commitment to sound operations, ongoing innovation, and open collaboration, we have established a competitive ICT portfolio of end-to-end solutions in telecom and enterprise networks, devices, and cloud technology and services. Our ICT solutions, products, and services are used in more than 170 countries and regions, serving over one-third of the world's population. With 180,000 employees, Huawei is committed to enabling the future information society, and building a Better Connected World. Huawei ranked 83th on the Global Fortune 500 based on its revenue in 2016. In 2016, the company’s revenue reached approximately USD 75.1 billion, with a 32% increase YOY and a solid increase in profits and cash flow.

As part of its overall investment strategy, Huawei supports innovation and contributions to the development of the economy in the countries where the group operates. Convinced that Europe and France in particular have a leading role to play on the world digital scene, Huawei is involved in the development of the digital sector and supports research and development in Europe. Huawei already has many R&D centers in place to meet market expectations.

The All-Digital Phase-Locked Loop (ADPLL) digital electronic circuit that are used in modern electronic

Communication systems like frequency synthesizer, modulator/demodulator is one of the principal research domains at the Huawei Nice Research Center in Sophia Antipolis.

With the fast evolution of 5G scenarios, important milestones in 5G research and development have been reached and standardization efforts are underway. We are working closely on ADPLL in order to get ready for the commercial launch of the next generation's mobile technology.

The aim of this internship is to leverage cutting edge research to improve the Base Band Digital section of ADPLL Synthesizers; Digital Time converters (DTCs), Time to Digital Converters, (TDC) ALL Digital Phase Frequency Detectors. The challenge is to correctly design and estimate electrical performances. This is an opportunity for R&D in a new advanced high-tech domain using digital processing and machine learning techniques.

The candidate will have the following responsibilities during the internship:

* Study start of the art (e.g. papers from top universities worldwide)
* Design Base Band circuits for Digital Phase Detection
* Be responsible of top level validation of such circuits in the complete system Understand and root cause the observed issues
* Develop the layout for silicon foundry and take care of electrical characterization of circuits .

The candidate will be closely integrated into a team of RF and Synthesizers experts and will thus benefit from the knowledge and experience of the inter-disciplinary team based in Sophia Antipolis.

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| Position Requirements | •knowledge in semiconductor physics, technology of CMOS devices. •knowledge of microelectronics and electronics: analog circuit design and some experience in digital circuit design. •Some experience with the VLSI design techniques and the use of EDA design tools (e.g. Cadence IC, Synopsys) are desirable, basic Matlab and Verilog. It is expected that the candidate will have excellent communication skills, a strong motivation and work autonomously |